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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/815,465	03/31/2004	Shawn L. Lloyd	884.C22US1	6387

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EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 05/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/815,465	LLOYD ET AL.	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27 and 32-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27 and 32-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Drawings

1. The drawings are objected to because the reference numerals are not clear and legible. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claim 1 is objected to because of the following informalities:

A. The limitations as recited in claim 1, line 10 include "the second height greater than the first height".

However, se described in the specification (see Fig. 2, pp. 6), the h2 is smaller than h1.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-7, 11-14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kelly et al. (US Pat. 5798567) in view of Miyazawa (US Pat. App. Pub. No. 2002/0182842).

Regarding claims 1-7, 11 and 16 Kelly et al. disclose an integrated circuit (IC) device/package/assembly having a ball grid array (BGA) semiconductor device (see 61/63 in Fig. 5), the device/package comprising:

- a substrate including a first/bottom major surface (63 and 68 respectively in Fig. 5) including a plurality of portions of conductive pads/lands (CP/CL) including first, second and third portions (see pads under solder balls and various components – not numerically referenced in Fig. 5) and a second/top major surface
- a plurality of passive/discrete components including more than three components having substantially the same dimensions/height, the components comprising capacitors (67 in Fig. 5) being attached using conventional surface mount attachment to respective second and third portions of the CL/CP on the first/bottom surface
- a plurality/array of solder balls/spacers (see 69 in Fig. 5) having a first height/h1 with respect to the first/bottom major surface of the BGA device being attached to respective first portions of the CP/CL on a printed circuit board (PCB)/substrate (71 in Fig. 5),
- the passive/discrete components further having a second height/h2 with respect to the first/bottom surface, the h2 being smaller than the h1

(Fig. 5; Col. 4, lines 6-66; Col. 2-5).

Kelly et al. fail to teach at least one component being a sacrificial component (SC) from the passive/discrete components being attached to the first major surface wherein the SC includes a fuse.

Miyazawa teaches a module/ICP having a variety of plurality of electronic parts/components on top and bottom surface of an interconnect substrate/board (see 20, 22, 42, etc. on 10 in Fig. 1B), the module/ICP further comprising:

- the electronic parts/components using surface mount attachment and including active components such as an IC device and passive/discrete components such as capacitor, fuse/SC (see 22 in Fig. 1B; section 0079) the interconnect substrate/board having an array/plurality of first, second and third portions of the interconnect patterns/CP/CL, etc. (see 16 under various components in Fig. 1A/1B)
- the SC/fuse being positioned between two solder contacts on respective/third portion of the interconnect patterns/CP/CL (see 30/32 in Fig. 1A/1B), the other passive/discrete components being positioned on the respective/second portions of the interconnect patterns/CP/CL and
- the SC comprising a body, the body having a first surface/bottom including two solder contacts at the sides/ends of the SC and a second/top surface substantially parallel with the first/bottom surface devoid of the CL/CP/conductor (see 22 in Fig. 1B; sections 0079-0081)

(Fig. 1A-3; sections 0073-0122).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate at least one SC including a fuse as taught by

Miyazawa so that the desired electrical performance/reliability, device integration and noise reduction can be achieved in Kelly et al's device.

Regarding claims 12-14, Kelly et al. teach substantially the entire claimed structure as applied to claims 1 and 11 above, except at least one discrete component has a first height and the at least one SC has a second height greater than the first height.

Miyazawa further teaches the plurality of passive/discrete components including the SC where the components have different heights from the mounting surface of the interconnect substrate/board (see 20, 22, etc. in Fig. 1A/1B). Such configuration of the components on the ICP would yield the placement of the components including the SC being positioned to prevent the other/discrete having smaller height from contacting the PCB surface opposite to the mounting surface and provides the second/top body surface positioned near the PCB being devoid of electrically conductive material.

Furthermore, determination of component parameters such as length, width, height, spacing, number of functional/non-functional components, number of CL/CP, etc. in a final assembly of the ICP is a subject of routing optimization and experimentation to achieve the desired spacing/gap between two substrates or that among the adjacent components, circuit performance, noise reduction, repair/inspection capability and overall package size/weight/dimensions.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate at least one discrete component has a first height and the at least one SC has a second height greater than the first height as taught by Miyazawa so that the desired clearance between the adjacent substrates can be achieved to prevent the other components/discrete components impacting another surface/PCB and to improve the repair/inspection, electrical performance and reliability in Kelly et al's device.

5. Claims 8-10, 17-20, 32, 33 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kelly et al. (US Pat. 5798567) and Miyazawa (US Pat. App. Pub. No. 2002/0182842) as applied to claims 1-7 above, and further in view of Hatagishi (US Pat. 4869972).

Regarding claims 8-10, Kelly et al. and Miyazawa teach substantially the entire method as applied to claims 1-7 above, except the SC/fuse comprising a C-shaped conductor wherein the fuse is embedded/molded within the body of the SC, the body being an insulative material.

Hatagishi discloses a fuse/SC structure (see A/B in Fig. 1-3) wherein the fuse/SC (1-3 in Fig. 1 and 2) comprises:

- a first and second major surfaces (see side surfaces 7/9 in Fig. 2) including first and second solderable surfaces (see 9 in Fig. 2)

- the fuse (see 1 and 2 in Fig. 2 and 3) being positioned between the first and the second solderable surfaces which are electrically connected to one another and being fixed/embedded/molded within an insulating/plastic casing/body/non-conductive block (7 in Fig. 3; Col. 3, line 12) such that the top/other surface is devoid of material other than the substantially insulative/nonconductive material (see Fig. 3)
- the fuse/SC comprising a conventional C/U shaped conductor having two contacts/free ends (see 9/3/2 in Fig. 2 and 3) to provide the desired electrical connection to respective contact sites (see 3/9 in Fig. 2 and 3), the fuse/SC further having a low heat generation and longer service life

(Col. 2, line 11- Col. 3, line 45).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate fuse comprising a C-shaped conductor wherein the fuse is embedded/molded within the body of the SC, the body being an insulative material as taught by Hatagishi so that the heat generation can be reduced the electrical performance/reliability can be improved in Kelly et al's device.

Regarding claims 17-20, Kelly et al., Miyazawa and Hatagishi teach substantially the entire method as applied to claims 1-11 above.

Regarding claims 32, 33 and 35, Kelly et al., Miyazawa and Hatagishi teach substantially the entire claimed structure as applied to claims 1-11 above.

6. Claims 15, 21-27 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kelly et al. (US Pat. 5798567) and Miyazawa (US Pat. App. Pub. No. 2002/0182842) as applied to claims 1-7 above, and further in view of Hatagishi (US Pat. 4869972) and Sugita et al. (US Pat. 5068706).

Regarding claim 15, Kelly et al., Miyazawa and Hatagishi teach substantially the entire claimed structure as applied to claims 1-7 and 11 above, wherein Kelly et al. further teach the PCB further comprising ground and power planes (see the planes on 71 being contacted by solder balls connected to ground via 75 and power via 73; Col. 4, lines 17-52), but fail to teach at least one non operational SC being positioned with respect to the PCB.

Sugita et al. teach an ICP having a variety of fuse/SC configurations wherein the fuse/SC is in non operational state/blown configuration (see Fig. 6C, 81 in Fig. 9B, etc.).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate at least one non operational SC being positioned with respect to the PCB to prevent the at least one discrete component from contacting the ground and power planes of the PCB as taught by Sugita et al. so that breakage

of functional components can be prevented and the electrical performance/reliability can be improved in Miyazawa, Hatagishi and Kelly et al's device.

Regarding claims 21-27, Kelly et al., Miyazawa, Hatagishi and Sugita et al. teach substantially the entire claimed structure as applied to claims 1-7 and 11-15 above.

Regarding claim 34, Kelly et al., Miyazawa, Hatagishi and Sugita et al. teach substantially the entire claimed structure as applied to claims 1-11 and 32 above.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAN or Public PAG. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAG system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Nitin Parekh

NP

05-24-05

NITIN PAREKH

PRIMARY EXAMINER

Technology Center 2800